EE101 Lecture 9, Feb 5 2019

Midterm Exam on Feb 7

1 page of formulas, tables & calculator allowed.

coverage (up to Jan 31)

- Ohm's Law
- KCL } for calculation of voltages (node, branch)
- KVL } and currents (mesh, branch), Power (+, −)
- Equivalent circuit (Thevenin's, Norton's)
- Diodes, Diode circuits (including LEDs)
- Op Amp circuit.

5 problems for 95 min examination

HW #5 (for Quiz 5)

[1] Prob 4.13

[2] 4.18

[3] 4.20

[4] 4.25

[5] 4.35

[6] 4.43

[7] m 4.3

[8] m 4.4

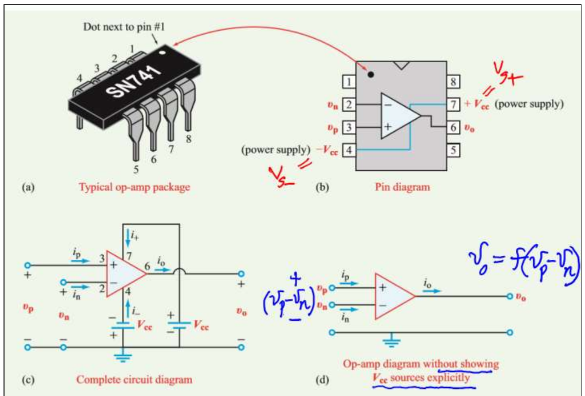


Figure 4-2: Operational amplifier.

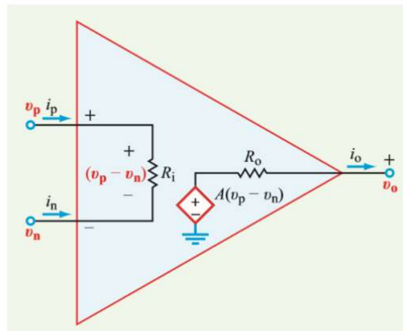


Figure 4-6: Equivalent circuit model for an op amp operating in the linear range ($v_o \leq |V_{cc}|$). Voltages v_p, v_n, and v_o are referenced to ground.

Table 4-1: Characteristics and typical ranges of op-amp parameters. The rightmost column represents the values assumed by the ideal op-amp model.

Op-Amp Characteristics	Parameter	Typical Range	Ideal Op Amp
• Linear input-output response	Open-loop gain A	10^4 to 10^8 (V/V)	∞
• High input resistance	Input resistance R_i	10^6 to 10^{13} Ω	∞ Ω
• Low output resistance	Output resistance R_o	1 to 100 Ω	0 Ω
• Very high gain	Supply voltage V_{cc}	5 to 24 V	As specified by manufacturer

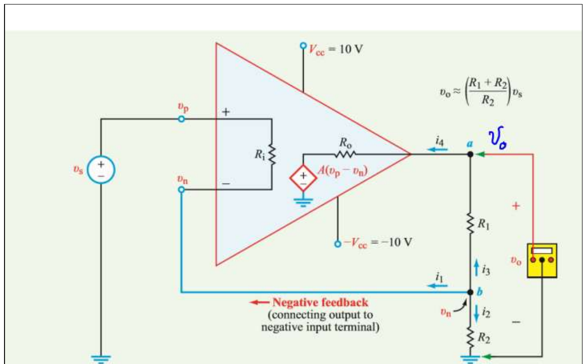
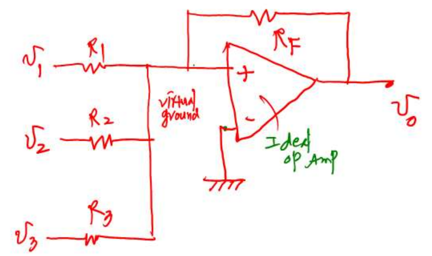


Figure 4-7: Noninverting amplifier circuit of Example 4-1.



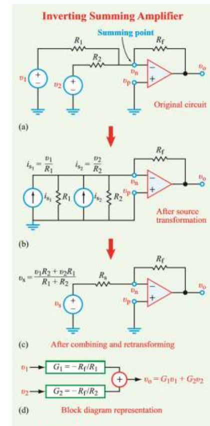
If $R_F = 3\,K\Omega,\ R_1 = 15\,K\Omega,\ R_2 = 10\,K\Omega,\ R_3 = 6\,K\Omega$

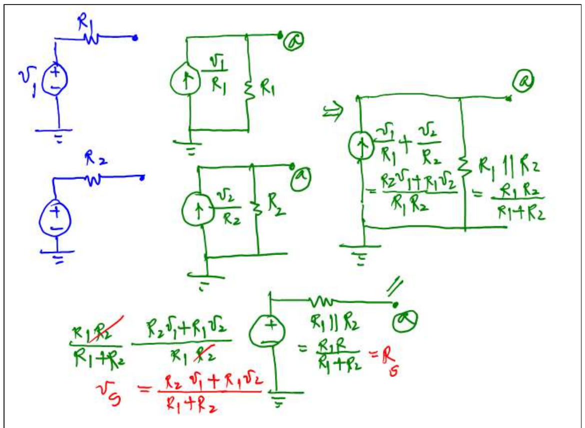
then $v_0 = -\left(\frac{R_F}{R_1} v_1 + \frac{R_F}{R_2} v_2 + \frac{R_F}{R_3}\right)$

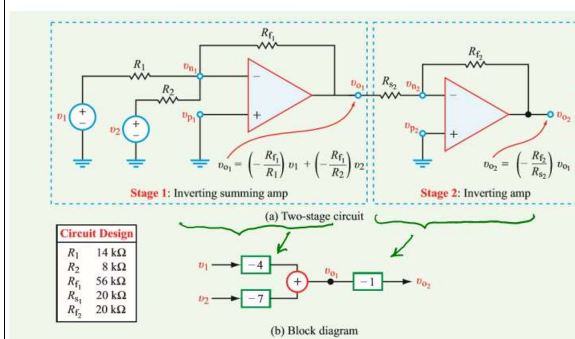
-(final score)

$= -(0.2\, v_1 + 0.3\, v_2 + 0.5\, v_3)$

Quiz Midterm final exam

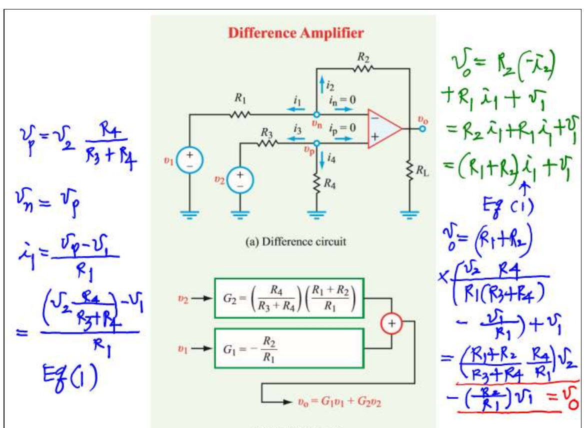






Circuit Design	
R_1	14 kΩ
R_2	8 kΩ
R_{f_1}	56 kΩ
R_{s_2}	20 kΩ
R_{f_2}	20 kΩ

Figure 4-14: Two-stage circuit realization of $v_o = 4v_1 + 7v_2$.



4-7 Voltage Follower/Buffer

4-7.1 No Buffer

In electronic circuits, we often need to incorporate the functionality of a relatively simple (but important) circuit that serves to isolate the input source from variations in the load resistance R_L. Such a circuit is called a ***voltage follower***, ***buffer***, or ***unity gain amplifier***. To appreciate the utility of the voltage follower, let us first examine the circuit shown in Fig. 4-17(a). A source input circuit represented by its Thévenin equivalent (v_s, R_s), is connected to a load R_L. The output voltage is

$$v_o = \frac{v_s R_L}{R_s + R_L} \quad \text{(without voltage follower)}, \qquad (4.45)$$

which obviously is dependent on both R_s and R_L, so if the load resistance R_L changes, so will the output voltage v_o.

4-7.2 With Op-Amp Buffer

In contrast, when the op-amp voltage follower circuit shown in Fig. 4-17(b) is inserted in between the source circuit and the load, the output voltage becomes completely independent of both R_s and R_L. Because $i_p = 0$, it follows that $v_p = v_s$. Furthermore, in view of the op-amp constraint $v_p = v_n$ and because the output node is connected directly to v_n, it follows that

$$v_o = v_p = v_s \quad \text{(with voltage follower)}, \qquad (4.46)$$

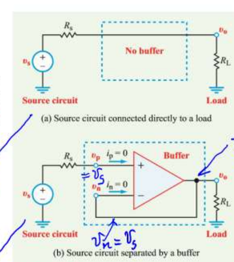


Figure 4-17: The voltage follower provides no voltage gain ($v_o = v_s$), but it insulates the input circuit from the load.

► When designing and building a multistage circuit, designers usually insert buffers between adjacent stages, which allows them to design each stage separately and then cascade them all together with buffers in between them. ◄

Basic Rules of Op-Amp Circuits

(1) KCL and KVL always apply everywhere in the circuit, but KCL is inapplicable at the output node when applying the ideal op-amp model. All other circuit-analysis tools can be applied to op-amp circuits.

(2) The op amp will operate in the linear range so long as $|v_o| < |V_{cc}|$.

(3) The ideal op-amp model assumes that the source resistance R_s (connected to terminals v_p or v_n) is much smaller than the op-amp input resistance R_i (which usually is no less than 10 MΩ), and the load resistance R_L is much larger than the op-amp output resistance R_o (which is on the order of tens of ohms).

(4) The ideal op-amp constraints are $i_p = i_n = 0$ and $v_p = v_n$.

4.11 Determine the output voltage for the circuit in **Fig. P4.11** and specify the linear range for v_s, given that $V_{cc} = 15$ V and $V_0 = 0$.

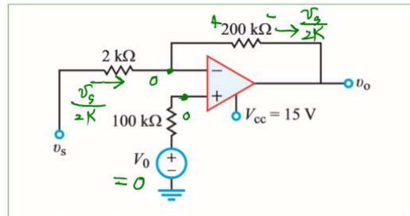


Figure P4.11: Circuit for Problems 4.11 and 4.12.

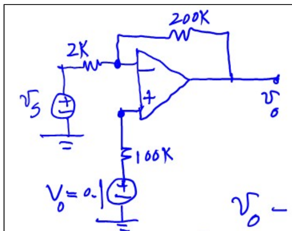
$v_o = -\frac{v_s}{2K} \times 200K \doteq -100 v_s$

$v_{o\,max} \doteq 15V$

$v_{o\,min} = -15V$

$\Rightarrow |v_s| < 150$ [mV]

4.12 Repeat Problem 4.11 for $V_0 = 0.1$ V.



$v_o = -\left(200K \cdot \frac{v_s - 0.1}{2K}\right)$

$= -100(v_s - 0.1)$

$v_o - 10 = -100 v_s$

$v_{o\,max} = 15V$

$v_{o\,min} = -15V$

$5 = -100 v_s, \quad v_s \geq -50mV$

$-25 = -100 v_s, \quad v_s \leq 250mV$

$G_i = \frac{i_L}{i_s}$

***(b)** If $R_L = 12$ kΩ, choose R_f so that $G_i = -15$.

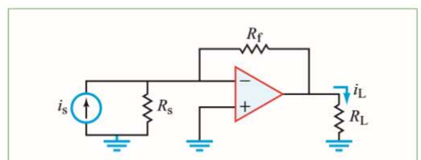
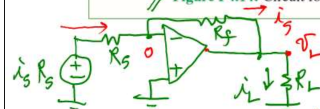


Figure P4.14: Circuit for Problem 4.14.



$v_L = -R_f i_s$

$i_L = -\frac{R_f}{R_L} i_s$ (180K)

$-15 = G_i = \frac{i_L}{i_s} = -\frac{R_f}{R_L}$, $R_L = 12K$

4.17 Determine v_o across the 10 kΩ resistor in the circuit of **Fig. P4.17**.

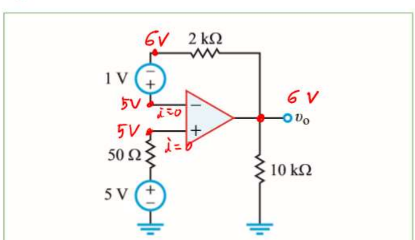


Figure P4.17: Circuit for Problem 4.17.

4.22 The circuit in **Fig. P4.22** uses a potentiometer whose total resistance is $R = 10$ kΩ with the upper section being βR and the bottom section $(1-\beta)R$. The stylus can change β from 0 to 0.9. Obtain an expression for $G = v_o/v_s$ in terms of β and evaluate the range of G (as β is varied over its own allowable range).

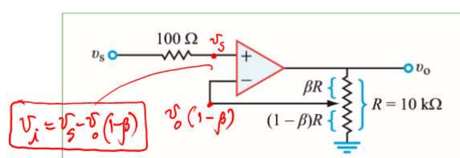


Figure P4.22: Circuit for Problem 4.22.

$v_o = A v_i = A[v_s - v_o(1-\beta)]$

$A v_s = v_o(1 + (1-\beta)A)$

$\frac{v_o}{v_s} = G = \frac{A}{1+(1-\beta)A} = \frac{1}{1-\beta}$ (when $A = \infty$)

4.23 For the circuit in **Fig. P4.23**, obtain an expression for voltage gain $G = \upsilon_o/\upsilon_s$.

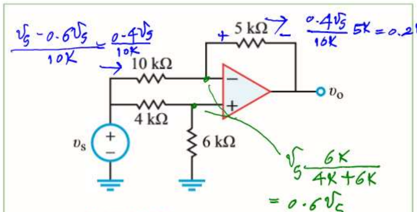


Figure P4.23: Circuit for Problem 4.23.

$v_o = -0.2v_s + 0.6v_s = 0.4 v_s$

$\frac{v_o}{v_s} = 0.4 = G$

***4.24** Find the value of υ_o in the circuit in **Fig. P4.24**.

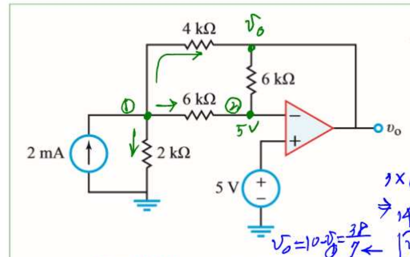


Figure P4.24: Circuit for Problem 4.24.