EE 101 Lecture 10, Feb 12, 2019

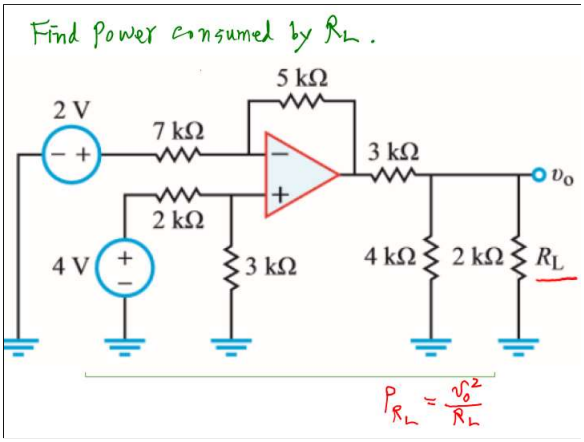
Quiz 4 avg = 7.22
σ = 1.97

Midterm Avg = 73.96
(101 students) σ = 16.00

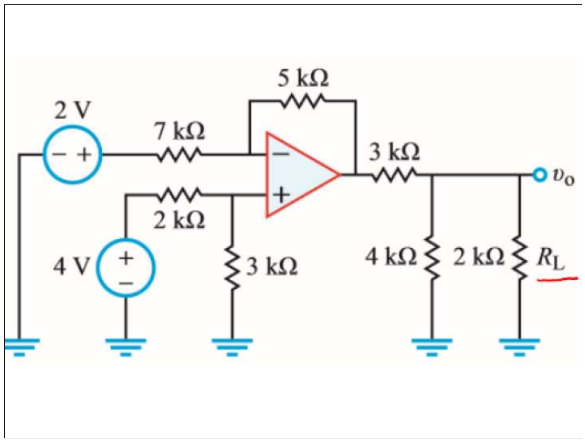
HW #6 (for Quiz 6)

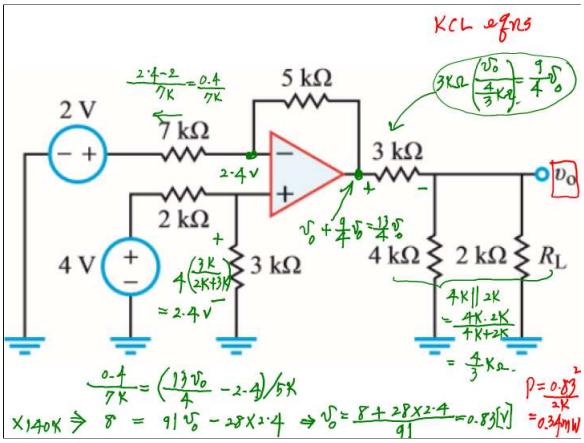
[1] Prob 5.1
[2] 5.3
[3] 5.4
[4] 5.15
[5] 5.16
[6] 5.17
[7] 5.18
[8] 5.19

Find Power consumed by R_L.



$P_{R_L} = \frac{v_o^2}{R_L}$





$\frac{0.4}{7K} = \left(\frac{11}{4}v_o - 2.4\right)/5K$

$\times 140K \Rightarrow 8 = 91 v_o - 28 \times 2.4 \Rightarrow v_o = \frac{8 + 28 \times 2.4}{91} = 0.83[V]$

$P = \frac{0.83^2}{2K} = 0.34mW$

*4.50 Relate the output voltage v_o in Fig. P4.50 to v_s.

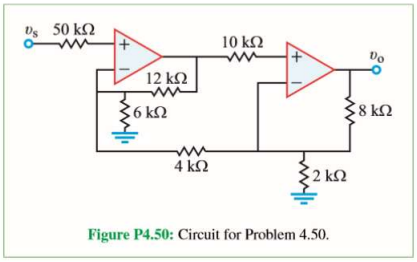
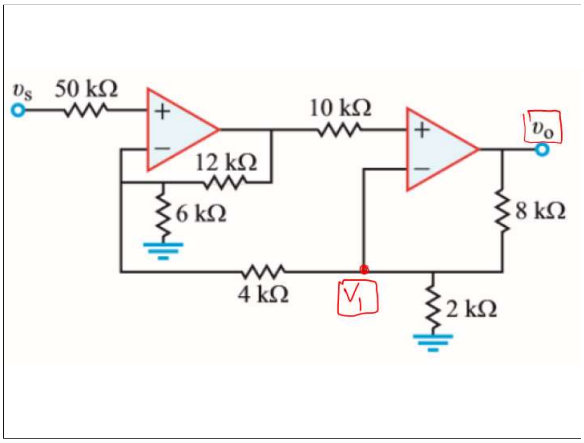
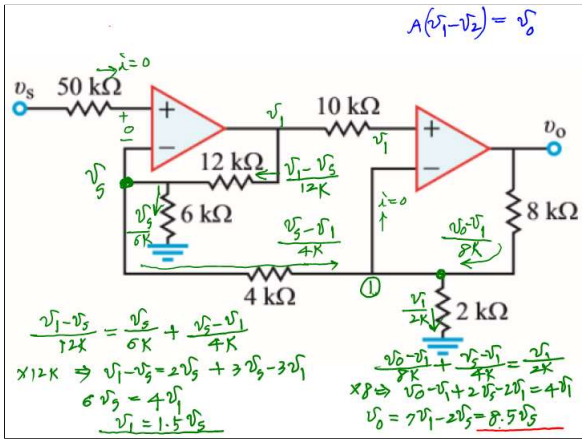


Figure P4.50: Circuit for Problem 4.50.





m4.1 Ideal Op-Amp Model:

(a) Determine a general expression for v_{out} in terms of the resistor values and i_s for the circuit of Fig. m4.1 (no Multisim or myDAQ for this part).

(b) Find V_{out} for these specific component values: $R_1 = 3.3$ kΩ, $R_2 = 4.7$ kΩ, $R_3 = 1.0$ kΩ, and $I_s = 1.84$ mA.

(c) Replace R_2 with a potentiometer. Use myDAQ and the potentiometer to determine V_{out} for each of the following values of R_2: 2.5 kΩ, 10 kΩ, and 25 kΩ.

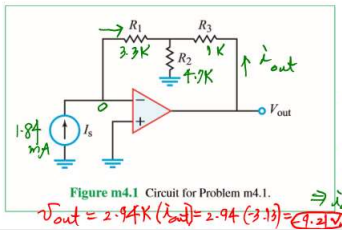


Figure m4.1 Circuit for Problem m4.1.

$3.3K \| 4.7K = \frac{3.3K \times 4.7K}{3.3K + 4.7K} = \frac{3.3K \times 4.7K}{8K} = 1.94K\Omega$

$i_{out} = \frac{v_{out}}{(1+1.94)K}$

$i_{out} \frac{4.7K}{3.3K + 4.7K} = -1.84mA$

$\Rightarrow i_{out} = -1.84mA \frac{8}{4.7} = -3.13\,mA$

$v_{out} = 2.94K(i_{out}) = 2.94(-3.13) = -9.2V$

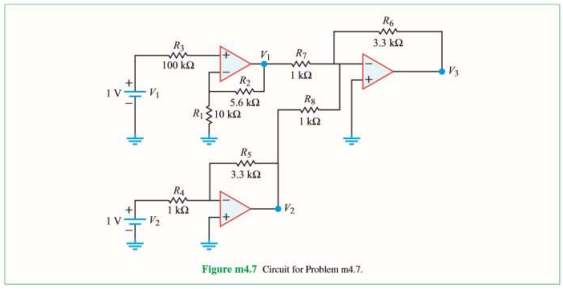
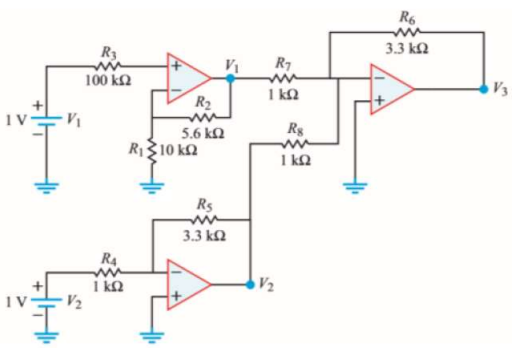


Figure m4.7 Circuit for Problem m4.7.

m4.7 Cascaded Op Amps: Find the voltage at each of the op amp outputs, V_1, V_2, V_3



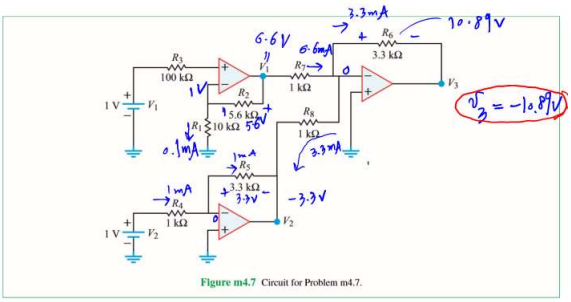


Figure m4.7 Circuit for Problem m4.7.

m4.7 Cascaded Op Amps: Find the voltage at each of the three op-amp outputs in the circuit of Fig. m4.7.

[prob] Express v_o in terms of v_1 & v_2

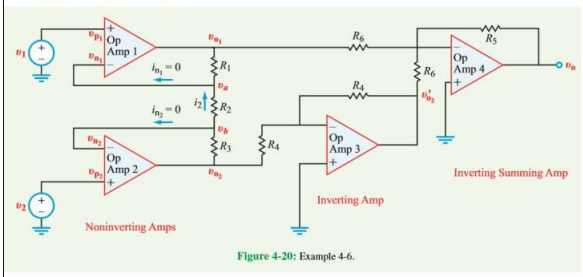
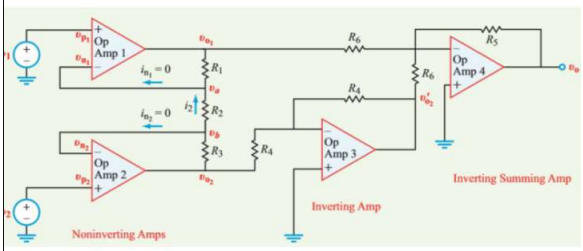
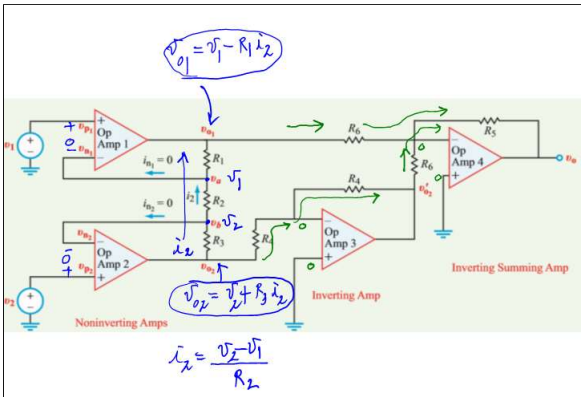


Figure 4-20: Example 4-6.





Since $i_{n_1} = i_{n_2} = 0$ (op-amp current constraint),

$$i_2 = \frac{v_b - v_a}{R_2} = \frac{v_2 - v_1}{R_2},$$

and

$$v_{o_2} - v_{o_1} = i_2(R_1 + R_2 + R_3) = \left(\frac{R_1 + R_2 + R_3}{R_2}\right)(v_2 - v_1). \quad (4.50)$$

Op amp 3 is a standard inverting amplifier, so we can use Table 4-3(c) to obtain

$$v'_{o_2} = -\left(\frac{R_4}{R_4}\right) v_{o_2} = -v_{o_2}.$$

Op amp 4 is an inverting summing amplifier (Table 4-3(c)) with output

$$\begin{aligned} v_o &= -\frac{R_5}{R_6}(v_{o_1} + v'_{o_2}) \\ &= -\frac{R_5}{R_6}(v_{o_1} - v_{o_2}) \\ &= \frac{R_5}{R_6}(v_{o_2} - v_{o_1}) = R_5\left(\frac{R_1 + R_2 + R_3}{R_6 R_2}\right)(v_2 - v_1). \end{aligned} \quad (4.51)$$

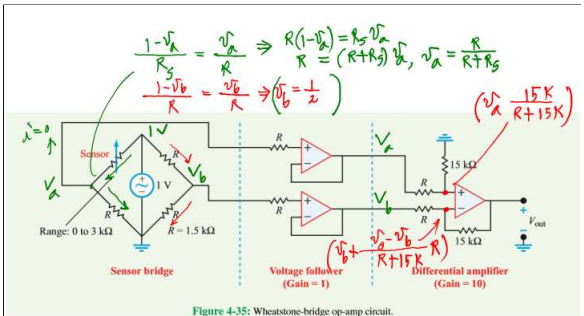
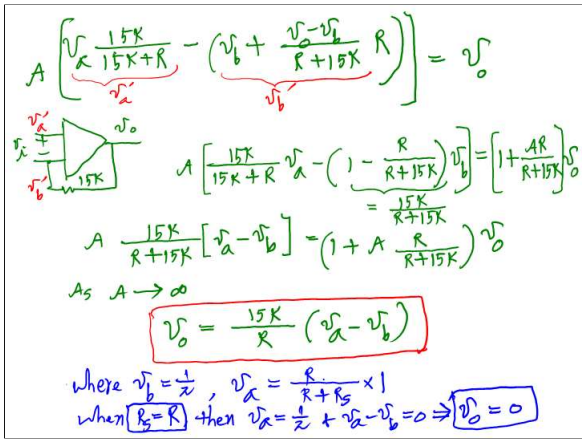


Figure 4-35: Wheatstone-bridge op-amp circuit.



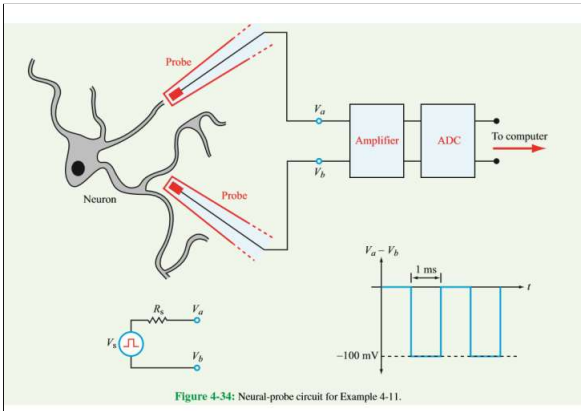


Figure 4-34: Neural-probe circuit for Example 4-11.

4-10 Digital-to-Analog Converters (DAC)

▶ A *digital-to-analog converter* (DAC) is a circuit that transforms a digital sequence presented to its input into an analog output voltage whose magnitude is proportional to the decimal value of the input signal. ◀

An n-bit digital signal is described by the sequence $[V_1 V_2 V_3 \ldots V_n]$, where V_1 is called the *most significant bit* (MSB) and V_n is the *least significant bit* (LSB). Voltages V_1 through V_n can each assume only two possible states—either a 0 or a 1. When a bit is in the 1 state, its decimal value is 2^m, where m depends on the location of that bit in the sequence. For the most significant bit (V_1), its decimal value is $2^{(n-1)}$; for V_2 it is $2^{(n-2)}$; and so on. The decimal value of the least significant bit is $2^{n-n} = 2^0 = 1$, when that bit is in state 1. Any bit in state 0 has a decimal value of 0. Table 4-4 illustrates the correspondence between the binary sequences of a 4-bit digital signal and their decimal values. The binary sequences start at [0000] and end at [1111], representing 16 decimal values extending from 0 to 15 and inclusive of both ends. To do so, the DAC in Fig. 4-24 has to sum V_1 to V_n after weighting each by a factor equal to its decimal value. Thus, for a 4-bit digital sequence, for example, the output voltage of the DAC has to be related to the input by

$$V_{\text{out}} = G(2^{4-1}V_1 + 2^{4-2}V_2 + 2^{4-3}V_3 + 2^{4-4}V_4)$$
$$= G(8V_1 + 4V_2 + 2V_3 + V_4), \qquad (4.57)$$

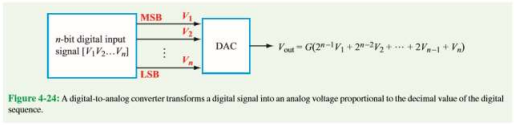


Figure 4-24: A digital-to-analog converter transforms a digital signal into an analog voltage proportional to the decimal value of the digital sequence.

Table 4-4: Correspondence between binary sequence and decimal value for a 4-bit digital signal and output of a DAC with $G = -0.5$.

$V_1V_2V_3V_4$	Decimal Value	DAC Output (V)
0000	0	0
0001	1	−0.5
0010	2	−1
0011	3	−1.5
0100	4	−2
0101	5	−2.5
0110	6	−3
0111	7	−3.5
1000	8	−4
1001	9	−4.5
1010	10	−5
1011	11	−5.5
1100	12	−6
1101	13	−6.5
1110	14	−7
1111	15	−7.5

to either Table 4-3(c) or Eq. (4.34) yields

$$V_{\text{out}} = -\frac{R_f}{R}V_1 - \frac{R_f}{2R}V_2 - \frac{R_f}{4R}V_3 - \frac{R_f}{8R}V_4$$
$$= \frac{-R_f}{8R}(8V_1 + 4V_2 + 2V_3 + V_4), \qquad (4.58)$$

which satisfies the relative weights given in Eq. (4.57). Also, in this case,

$$G = -\frac{R_f}{8R}. \qquad (4.59)$$

For $[V_1V_2V_3V_4] = [1111]$, $V_{\text{out}} = 15G$. By selecting $G = -0.5$ (corresponding to $R_f = 4R$), the output will vary from 0 to −7.5.

Example 4-8: *R–2R* Ladder

The circuit in Fig. 4-26(a) offers an alternative approach to realizing digital-to-analog conversion of a 4-bit signal. It is called an *R–2R* ladder, because all of the resistors of its

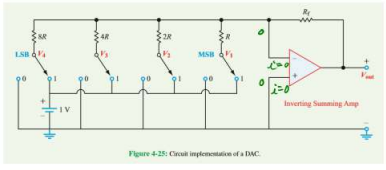


Figure 4-25: Circuit implementation of a DAC.

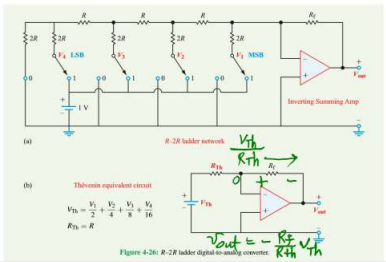
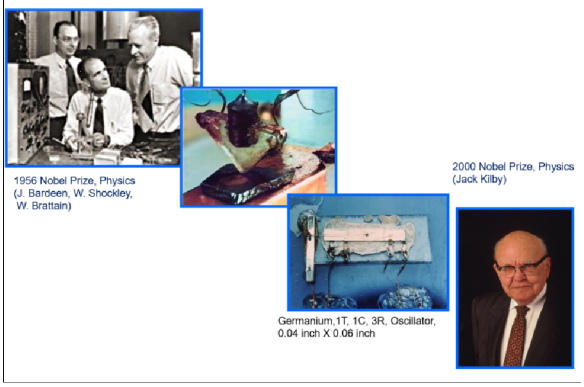


Figure 4-26: *R-2R* ladder digital-to-analog converter.

Transistor Invention (1948) to Integrated Circuit (1958)



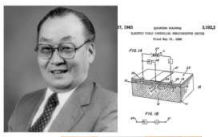
1956 Nobel Prize, Physics
(J. Bardeen, W. Shockley, W. Brattain)

2000 Nobel Prize, Physics
(Jack Kilby)

Germanium,1T, 1C, 3R, Oscillator, 0.04 inch X 0.06 inch

First Successful Operation of MOS Transistor

Dawon Kahng (May 4, 1931- May 13, 1992)



Simon Sze

- SNU (BS), Ohio State Univ. (Ph.D. 1959)
- Dr. Kahng, with M. Atalla, fabricated a MOSFET using a gate insulator formed from high quality SiO2 grown by a new high-pressure steam oxidation process at Bell Labs (1960)
- First successful demonstration of MOSFET was a major milestone in semiconductor technology
- Invented in 1967 a field effect memory, the first nonvolatile silicon memory (floating gate memory)
- Became Founding President of NEC, Princeton, NJ in 1988

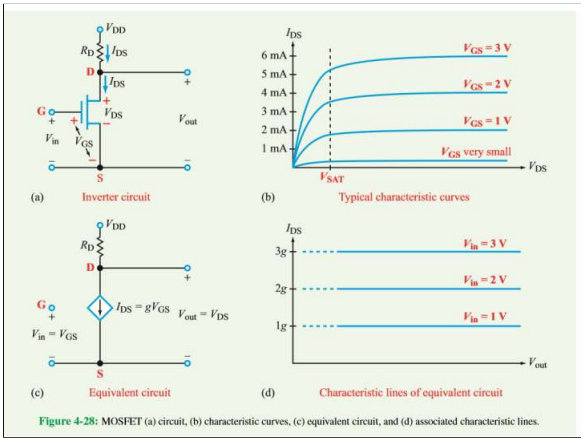


Figure 4-28: MOSFET (a) circuit, (b) characteristic curves, (c) equivalent circuit, and (d) associated characteristic lines.

4-11 The MOSFET as a Voltage-Controlled Current Source

In earlier sections, we demonstrated how op amps can be used to build buffers and amplifiers. We now examine how to realize the same outcome using MOSFETs. The simplest model of a ***MOSFET***, which stands for ***metal-oxide semiconductor field-effect transistor***, is shown in **Fig. 4-27(a)**. The vast majority of commercial computer processors are built with MOSFETs; as mentioned in Technology Brief 1 on nanotechnology, a 2010 Intel Core processor contains over 1 billion independent MOSFETs. A MOSFET has three terminals: the ***gate*** (G), the ***source*** (S), and the ***drain*** (D). Actually, it has a fourth terminal, namely its body (B), but we will ignore it for now because for many applications it is simply connected to the ground terminal. The circuit symbol for the MOSFET may look somewhat unusual, but it is actually a stylized depiction of the physical cross section of a real MOSFET. In a real MOSFET, the gate

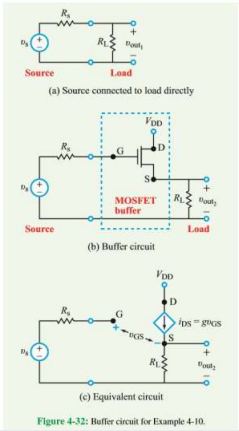


Figure 4-32: Buffer circuit for Example 4-10.

(b) With MOSFET Buffer

For the circuit in **Fig. 4-32(c)**, in which the MOSFET has been replaced with its equivalent circuit, KVL gives

$$-v_s + v_{GS} + v_{out_2} = 0.$$

Also,

$$\begin{aligned} v_{out_2} &= I_{DS} R_L \\ &= g R_L v_{GS}. \end{aligned}$$

Simultaneous solution of the two equations gives

$$\Rightarrow \quad v_{out_2} = \left(\frac{g R_L}{1 + g R_L} \right) v_s.$$

With $g = 10$ A/V and in order for v_{out_2} to be no less than $0.99 v_s$, it is necessary that

$$R_L \geq 9.9\ \Omega,$$

which is three orders of magnitude smaller than the requirement for the unbuffered circuit.

Section 4-11: MOSFET

4.59 In Example 4-9, we analyzed a common-source amplifier without a load resistance. Consider the amplifier in **Fig. P4.59**; it is identical to the circuit in **Fig. 4-31**, except that we have added a load resistor R_L. Obtain an expression for v_{out} as a function of v_s.

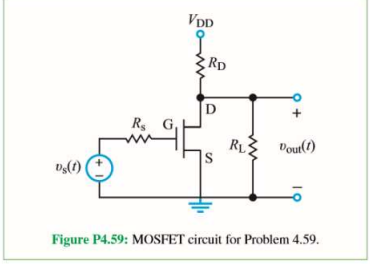
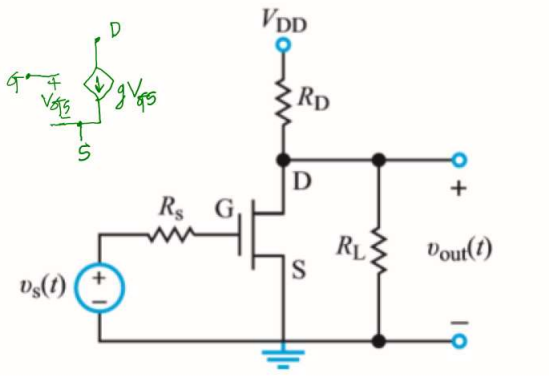


Figure P4.59: MOSFET circuit for Problem 4.59.



*4.60 Determine $v_{out}(t)$ as a function of $v_s(t)$ for the circuit in Fig. P4.60. Assume $V_{DD} = 2.5$ V.

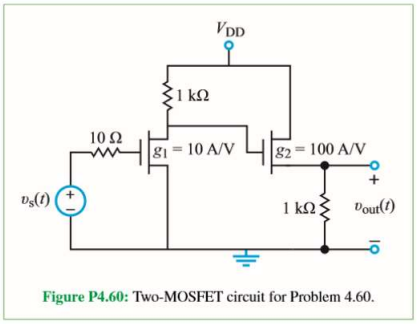
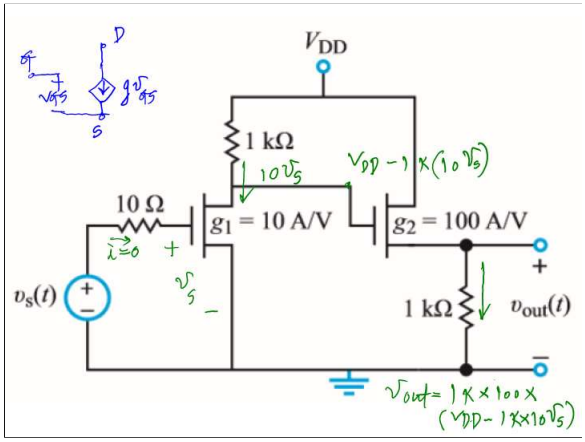
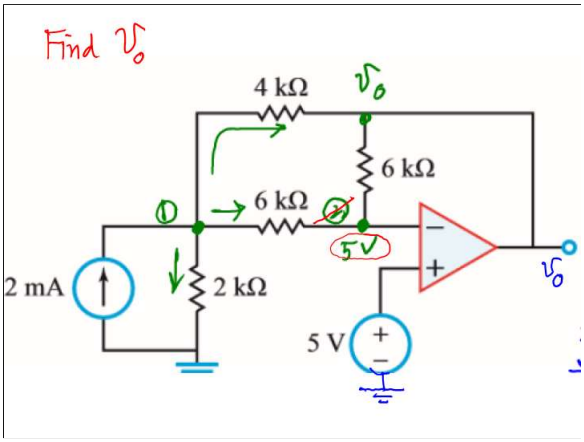


Figure P4.60: Two-MOSFET circuit for Problem 4.60.





*4.24 Find the value of v_o in the circuit in Fig. P4.24.

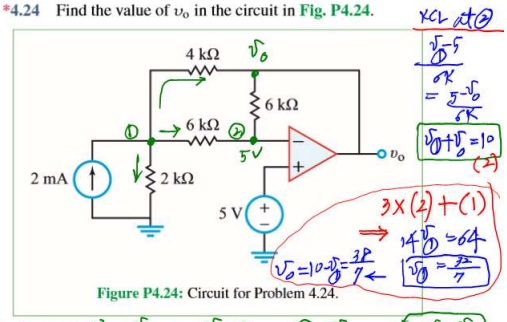


Figure P4.24: Circuit for Problem 4.24.

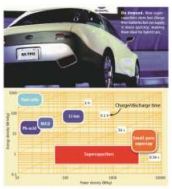
RC and RL First-Order Circuits

Contents

Objectives

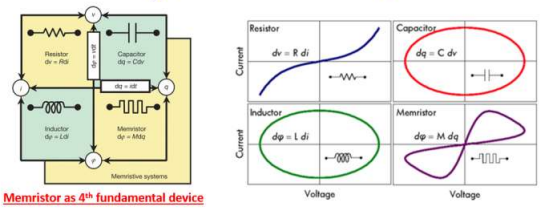
Learn to:

- Use mathematical functions to describe several types of nonperiodic waveforms.
- Define the electrical properties of a capacitor, including its i-v relationship and energy equation.
- Combine multiple capacitors when connected in series or in parallel.
- Define the electrical properties of an inductor, including its i-v relationship and energy equation.
- Combine multiple inductors when connected in series or in parallel.



Capacitors (C) and inductors (L) are *energy storage devices*, in contrast with resistors, which are energy dissipation devices. This chapter examines the behavior of *RC and RL circuits*, to be followed in Chapter 6 with an examination of RLC circuits.

- Analyze the transient responses of RC and RL circuits.
- Design RC op-amp circuits to perform differentiation and integration and related operations.
- Apply Multisim to analyze RC and RL circuits.



Memristor as 4th fundamental device

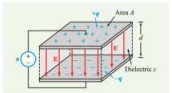


Figure 5-11: Parallel-plate capacitor with plates of area A, separated by a distance d, and filled with an insulating dielectric material of permittivity ε.

Table 5-2: Relative electrical permittivity of common insulators: $\varepsilon_r = \varepsilon/\varepsilon_0$ **and** $\varepsilon_0 = 8.854 \times 10^{-12}$ **F/m.**

Material	Relative Permittivity ε_r
Air (at sea level)	1.0006
Teflon	2.1
Polystyrene	2.6
Paper	2–4
Glass	4.5–10
Quartz	3.8–5
Bakelite	5
Mica	5.4–6
Porcelain	5.7

5-2 Capacitors

▸ When separated by an insulating medium, any two conducting bodies (regardless of their shapes and sizes) form a *capacitor*. A capacitor can store electric charge. ◂

The *parallel-plate capacitor* shown in Fig. 5-11 represents a simple configuration in which two identical conducting plates (each of area A) are separated by a distance d containing an insulating (dielectric) material of *electrical permittivity* ε. The permittivity of a material is usually referenced to that of free space, namely $\varepsilon_0 = 8.85 \times 10^{-12}$ farad/m (F/m). Hence, the *relative permittivity* of a material is defined as

$$\varepsilon_r = \frac{\varepsilon}{\varepsilon_0}. \tag{5.15}$$

When a dielectric material is subjected to an electric field, its atoms become partially polarized; i.e., the atom is rearranged into positive and negative domains. The *electric field* E induced in the space between the conducting plates is the result of the voltage v applied across the plates. The *electrical susceptibility* χ_e of a material is a measure of how susceptible that material is to electrical polarization. The permittivity ε and susceptibility χ_e are related by

$$\varepsilon = \varepsilon_0(1 + \chi_e). \tag{5.16}$$

In view of Eq. (5.15), the relative permittivity ε_r is given by

$$\varepsilon_r = \frac{\varepsilon}{\varepsilon_0} = 1 + \chi_e. \tag{5.17}$$

Free space contains no atoms; hence, its $\chi_e = 0$ and $\varepsilon_r = 1$. For air at sea level, $\varepsilon_r = 1.0006 \approx 1.0$. Table 5-2 provides typical values of ε_r for common types of insulators.

Returning to the parallel-plate capacitor, if a voltage source is connected across the two plates, as shown in Fig. 5-11, charge of equal and opposite polarity is transferred to the conducting surfaces. The plate connected to the $(+)$ terminal of the voltage source will accumulate charge $+q$, and charge $-q$ will accumulate on the other plate. The charges induce a nearly uniform electric field E in the dielectric medium, given by

$$E = \frac{q}{\varepsilon A}, \tag{5.18}$$

with the direction of E being from the plate with $+q$ to the plate with $-q$. Moreover, E, whose unit is V/m, is related to the voltage v through

$$E = \frac{v}{d} \quad \text{(V/m)} \qquad \text{(parallel-plate capacitor)}. \tag{5.19}$$

▸ For any capacitor, its *capacitance* C, measured in farads (F), is defined as the amount of charge q that its positive-polarity plate holds, normalized to the applied voltage responsible for that charge accumulation. ◂

Thus,

$$C = \frac{q}{v} \quad \text{(F)} \qquad \text{(any capacitor)}. \tag{5.20}$$

For the parallel-plate capacitor, combining Eqs. (5.18) and (5.19) leads to $q = \varepsilon Av/d$. Upon inserting this expression for q in Eq. (5.20), we have

$$C = \frac{\varepsilon A}{d} \qquad \text{(parallel-plate capacitor)}. \tag{5.21}$$

Even though the expression given by Eq. (5.21) is specific to the parallel-plate capacitor, the general tenor of the expression holds true for other geometrical configurations as well. In general, the capacitance C of any two-conductor system increases with the area of the conducting surfaces, decreases with the separation between them, and is directly proportional to ε of the insulating material. For example, the capacitance of a *coaxial capacitor* consisting of two concentric conducting cylinders of radii a and b (Fig. 5-12(a)) and separated by a dielectric material of permittivity ε is given by

$$C = \frac{2\pi\varepsilon\ell}{\ln(b/a)} \qquad \text{(coaxial capacitor)}, \tag{5.22}$$

where ℓ is the length of the capacitor and $\ln(b/a)$ is the natural logarithm of (b/a). The spacing between the cylinders is $(b-a)$; reducing this spacing, while holding b constant, requires reducing the ratio (b/a), which reduces the value of $\ln(b/a)$, thereby increasing the magnitude of C.

The *mica capacitor* shown in Fig. 5-12(b) consists of a stack of conducting plates, interleaved by sheets of mica (dielectric). The *plastic-foil capacitor* in Fig. 5-12(c) is constructed by rolling flexible conducting foils (separated by a plastic layer) into a spindle-like configuration. Small capacitors used in microcircuits typically have capacitances in the picofarad (10^{-12} F) to microfarad (10^{-6} F) range. Large capacitors used in power-transmission substations may have capacitors in the range of millifarads (10^{-3} F). Using thin-film polymers for the dielectric insulator and carbon nanotubes for the electrodes (terminals), a new type of capacitor (sometimes called a *supercapacitor* or *nanocapacitor*) was developed in the 1990s with the express goal of significantly increasing the amount of charge that the conductors can hold (at a specified voltage level). Such capacitors have capacitance values that are several orders of magnitude greater than conventional capacitors of comparable size. The new fabrication techniques have not only expanded the versatility of capacitors in electronic circuits, but they have also introduced the use of supercapacitors as energy-storage devices in many electronic applications (see Technology Brief 12: Supercapacitors).

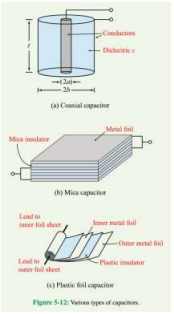


Figure 5-12: Various types of capacitors.

5-2.1 Electrical Properties of Capacitors

According to Eq. (5.20), $q = Cv$. Application of the standard definition for current (Eq. (1.3) provides the expression for the current i through a capacitor as

$$i = \frac{dq}{dt} = C\frac{dv}{dt}, \tag{5.23}$$

where the direction of i and the polarity of v are defined in accordance with the passive sign convention (Fig. 5-13).